

Sub 20 meV Schottky barriers in metal/MoTe₂ junctions

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Abstract. The newly emerging class of atomically-thin materials has shown a high potential for the realisation of novel electronic and optoelectronic components. Amongst this family, semiconducting transition metal dichalcogenides (TMDCs) are of particular interest. While their band gaps are compatible with those of conventional solid state devices, they present a wide range of exciting new properties that is bound to become a crucial ingredient in the future of electronics. To utilise these properties for the prospect of electronics in general, and long-wavelength-based photodetectors in particular, the Schottky barriers formed upon contact with a metal and the contact resistance that arises at these interfaces have to be measured and controlled. We present experimental evidence for the formation of Schottky barriers as low as 10 meV between MoTe₂ and metal electrodes. By varying the electrode work functions, we demonstrate that Fermi level pinning due to metal induced gap states at the interfaces occurs at 0.14 eV above the valence band maximum. In this configuration, thermionic emission is observed for the first time at temperatures between 40 K and 75 K. Finally, we discuss the ability to tune the barrier height using a gate electrode.

Keywords: MoTe₂, TMDCs, Schottky barriers, 2D materials, low temperature, thermionic emission

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1. Introduction

The emerging class of atomically thin materials has captured the interest of the research community due to the versatile physical phenomena that they exhibit[1, 2]. To name a few, the indirect to direct band gap transition as a function of layer number in atomically thin semiconductors[3], gate-controlled modulation of the band structure in few layer graphene[4] and phase structure transitions[5] hold the key to future innovations in electronic devices. Within this broad spectrum of materials, semiconducting transition metal dichalcogenides (TMDCs) are a major focal point for the wide scientific community working on fundamental and applied aspects of device physics due to their energy gaps of 1-2 eV.[6, 7] These gap values are ideally suited for electronics and optoelectronics, making TMDCs the prime candidates to replace bulk semiconductors in applications where added functionality, such as mechanical flexibility, is required. Atomically thin semiconductors also have the potential to readily form previously hard to access energy barriers, mostly in the few meV regime.[8] This feature stems from the wide variation in properties (*e.g.* work function and band gap values[6, 7]) found within the layered materials family. As such, by tailoring the energy barrier formed at the contacts to specific applications, TMDCs can be extremely valuable for light detection in the far infrared regime as internal photoemission diodes,[9] replacing other structures that are costly, or difficult to fabricate by any other means.

One approach to realise low energy barriers is by forming a Schottky junction between a TMDC and a metal. Several recent studies on few-layer TMDCs, such as MoS₂, WSe₂ and MoTe₂ have identified Schottky barriers as the primary contributors to the observed contact resistance.[10, 5, 11, 12, 13, 14, 15] Indeed, Guo *et al.* showed that metal induced gap states (MIGS) are the primary cause for barrier formation and that the Schottky barrier height (SBH) cannot be significantly altered by changing the work function of the contact metal.[10] In that work the formation of the Schottky barrier has been attributed mainly to the lack of dangling bonds normal to the crystallographic plane of TMDCs. The self terminating plane means that strong bonds between metal electrodes and the semiconductor cannot be easily formed, a fact that contributes to the increased contact resistance.[11] Experimentally, SBH values of 80 meV were reported with the thermionic emission process being dominant down to 100 K for MoTe₂[13, 14] and 60 K for MoS₂. [12] However, lower SBH values have, so far, not been achieved at cryogenic temperatures. At temperatures between 200 and 400 °C, a barrier height of 23 meV has been reported where the MoTe₂ flake is transferred onto pre-defined gold contacts, which may be due to a strain induced structural phase change from semiconducting 2H phase to a metallic 1T' phase at the contacts.[16]

Here we report the formation of ultra-low effective SBHs down to 10 meV on MoTe₂/metal structures, that is aided by Fermi level pinning at the interfaces. MoTe₂ is a TMDC with three different structural phases, the semiconducting 2H, and the semimetallic T_d and 1T' phases. The 2H phase consists of three hexagonal planes in a “sandwich” formation, with Te at the outer planes and Mo at the centre. These planes

are covalently bonded in a trigonal prismatic configuration that constitutes a single layer, and the layers are held together by van der Waals forces.[17, 18] The observed ultra-low effective SBHs in MoTe₂ play a minor role in the conduction at room temperature, but become significant at cryogenic temperatures and manifest in a strongly rectifying behaviour. By analysing the current-voltage characteristics of the conducting channel at different temperatures and various gate biases, we are able to extract its SBH and conductivity values. Within these systems, we find that thermionic emission persists as the dominant mechanism of transport at temperatures that range between 40 K and 75 K, whereas at higher temperatures ($T \geq 80$ K) other transport mechanisms become more prominent. By varying the electrode material, we show that MIGS pin the Fermi level at the interface at a level of 0.14 eV over the valence band maximum. Finally, we briefly discuss the modulation of the effective SBH with applied gate bias. Our results pave the way for the realisation of far infrared devices in TMDCs and provide insight on the mechanisms of transport in MoTe₂ at cryogenic temperatures.

2. Methods

Two terminal field effect devices, schematically shown in figure 1a were fabricated by mechanically exfoliating MoTe₂ flakes from a synthetic crystal (*HQ Graphene*) and transferring them onto highly doped silicon substrate with a high quality thermally grown oxide layer. The Si/SiO₂ serves as a global gate electrode and gate dielectric, respectively. Metal contacts were patterned using a regular electron beam lithography procedure immediately prior to metallisation. The devices were then thermally annealed for 2 hours in a H₂/Ar environment at 200 °C.

MoTe₂ flakes were characterised using Raman spectroscopy on a Renishaw Raman microspectrometer using a 532 nm laser. Atomic force microscopy (AFM) micrographs were obtained on an Innova AFM system (*Bruker Inc.*) working in the “tapping mode”, using a Nanosensors high-reflectivity probes operating at a resonance frequency of ~ 320 kHz, with a nominal radius of curvature of 10 nm or smaller. Once the quality of the flakes were established, the sample was loaded into a helium-3 cryostat, where the source-drain current *vs* source-drain voltage (I_{ds} - V_{ds}) response curves and the source-drain current *vs* gate-source voltage (I_{ds} - V_{gs}) were recorded at decreasing temperatures between 80 K and 40 K using a home-built electrical characterisation setup.

3. Results and Discussion

The devices, shown schematically in figure 1a, were characterised using Raman spectroscopy in ambient conditions to ensure that the flakes crystalline structure is the 2H phase (see figure 1b). The three peaks in the Raman spectrum (figure 1c), at ~ 170 cm⁻¹, ~ 230 cm⁻¹ and ~ 290 cm⁻¹ are the finger print modes of the 2H phase, namely the A_{1g} , E_{2g} and B_{2g} modes respectively.[20, 19, 21] The B_g (~ 163 cm⁻¹) and A_g (~ 260 cm⁻¹) peaks, which are associated with the 1T' phase[19] are absent indicating

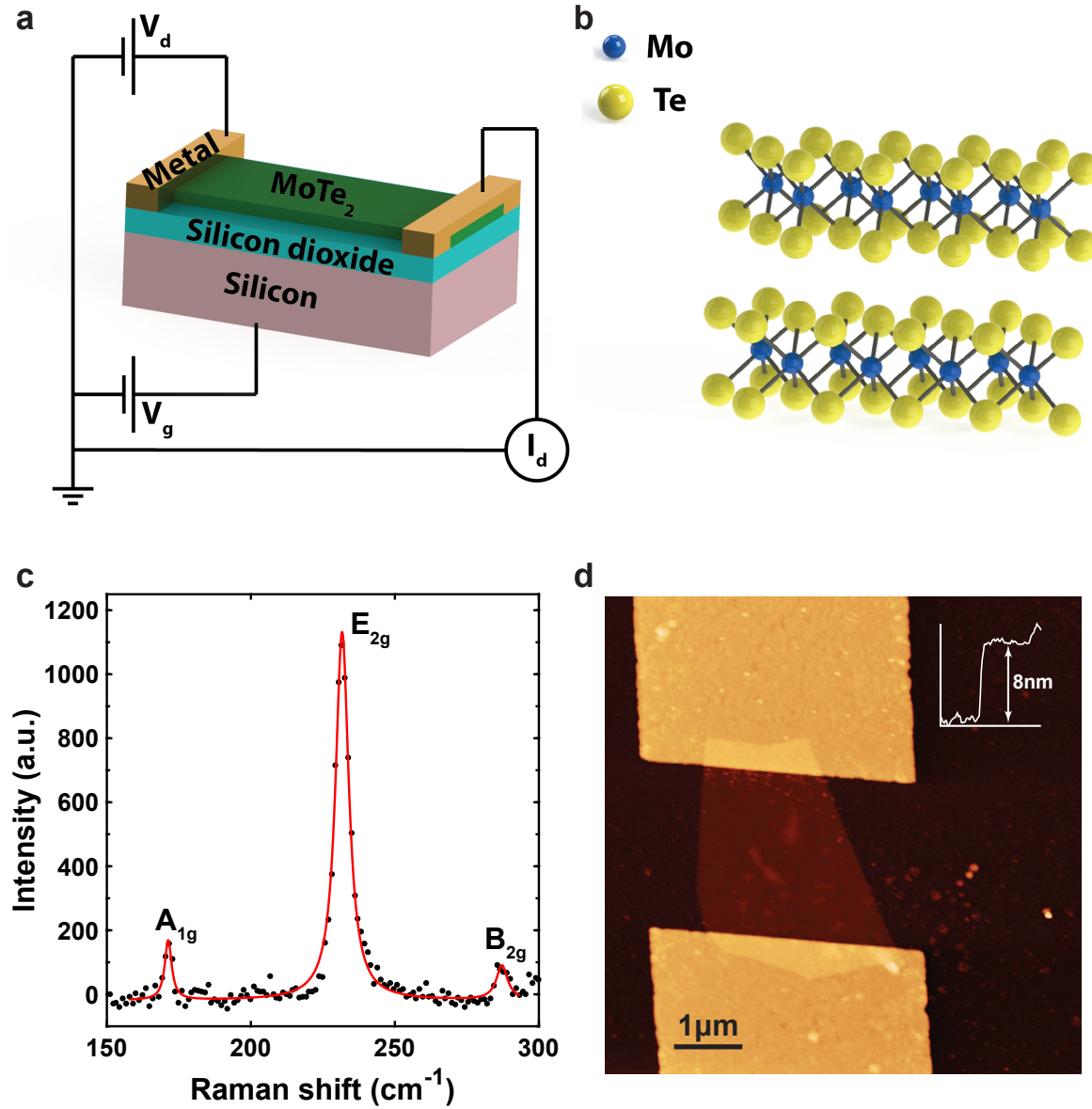


Figure 1. Material characterisation

a Schematic of an FET device using an MoTe₂ flake as the channel. The drain is the biased electrode and the current is measured at the source contact. The silicon layer acts as a global gate electrode with the silicon dioxide acting as the gate dielectric. **b** Crystal structure of 2H-MoTe₂ showing tellerium atoms (in yellow) covalently bonded to the molybdenum atoms (blue) in a “sandwich” formation. The covalently bound layers are held together by van der Waals forces. **c** Raman spectrum of typical flake showing A_{1g}, E_{2g} and B_{2g} peaks associated with few layer, 2H-MoTe₂. **d** AFM micrograph of a typical device with the height profile in the inset showing the flake has a thickness of 8 nm, equivalent to around 10 layers.

that the crystalline phase is indeed the semiconducting trigonal structure. As the T_d phase does not exist in room temperature, its Raman peaks are not considered here.[22]

The number of layers was determined from the thickness of the flake as measured

using atomic force microscopy (AFM). The device topography and structure are shown in the AFM micrograph (figure 1d). The cross section profile in the inset of the figure shows that the thickness of the flake is 8 nm, corresponding to 10 layers.[21] All the flakes used in this work were in the range of 5-10 layers.

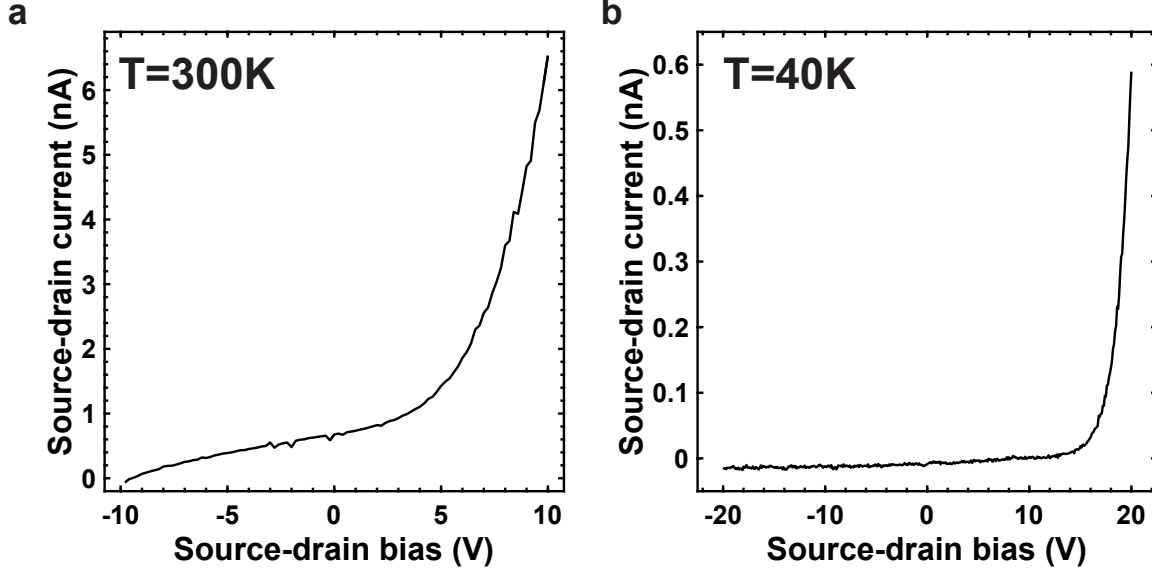


Figure 2. Response curves at different temperatures

a The response (I_{ds} - V_{ds}) curve for a device with Au contacts taken at room temperature while the device is in the “open” state at $V_{gs} = -40$ V. **b** The response curve for the same device taken at 40 K while the rest of the parameters are constant.

The few-layer MoTe₂ FET bears two identical metal contacts and should present current response characteristics that are symmetric about the zero source-drain bias ($V_{ds} = 0$ V). However, the response curve (I_{ds} - V_{ds}) shown in figure 2a is sub-linear and slightly rectifying, a trend that becomes more pronounced at lower temperatures (figure 2b). The increasingly rectifying response to V_{ds} with decreasing temperature is indicative of the formation of asymmetric Schottky barriers at the interfaces between the metal contacts and the semiconducting channel (see supplementary information section II online). While the semiconductor interface potential at the grounded (source) electrode is pinned by the bottom gate, and is effectively a fixed energy barrier, the electrostatic potential of the biased (drain) interface decreases the barrier height with forward bias.[23]

To gain further insights into the response characteristics of the devices, additional electrical characterisation was carried out in the temperature range from 80 K to 40 K. These measurements were performed at decreasing temperatures to avoid thermal emission of captured charge carriers which would significantly alter the barrier height. The source-drain current *vs* source-drain bias (I_{ds} - V_{ds}) response curves presented in figure 3a were measured on a device bearing Au contacts, using an applied gate bias (V_{gs}) of -40 V, which is in the devices “open” state. It is apparent that the device exhibits

a highly rectifying diode-like behaviour, which persists at lower temperatures. A graph on a semi-logarithmic scale, plotted in figure 3b, further emphasises the saturation of the source-drain current when the device is in reverse bias with respect to the source barrier. Other devices displayed similar trends and are shown in supplementary figure S1 online.

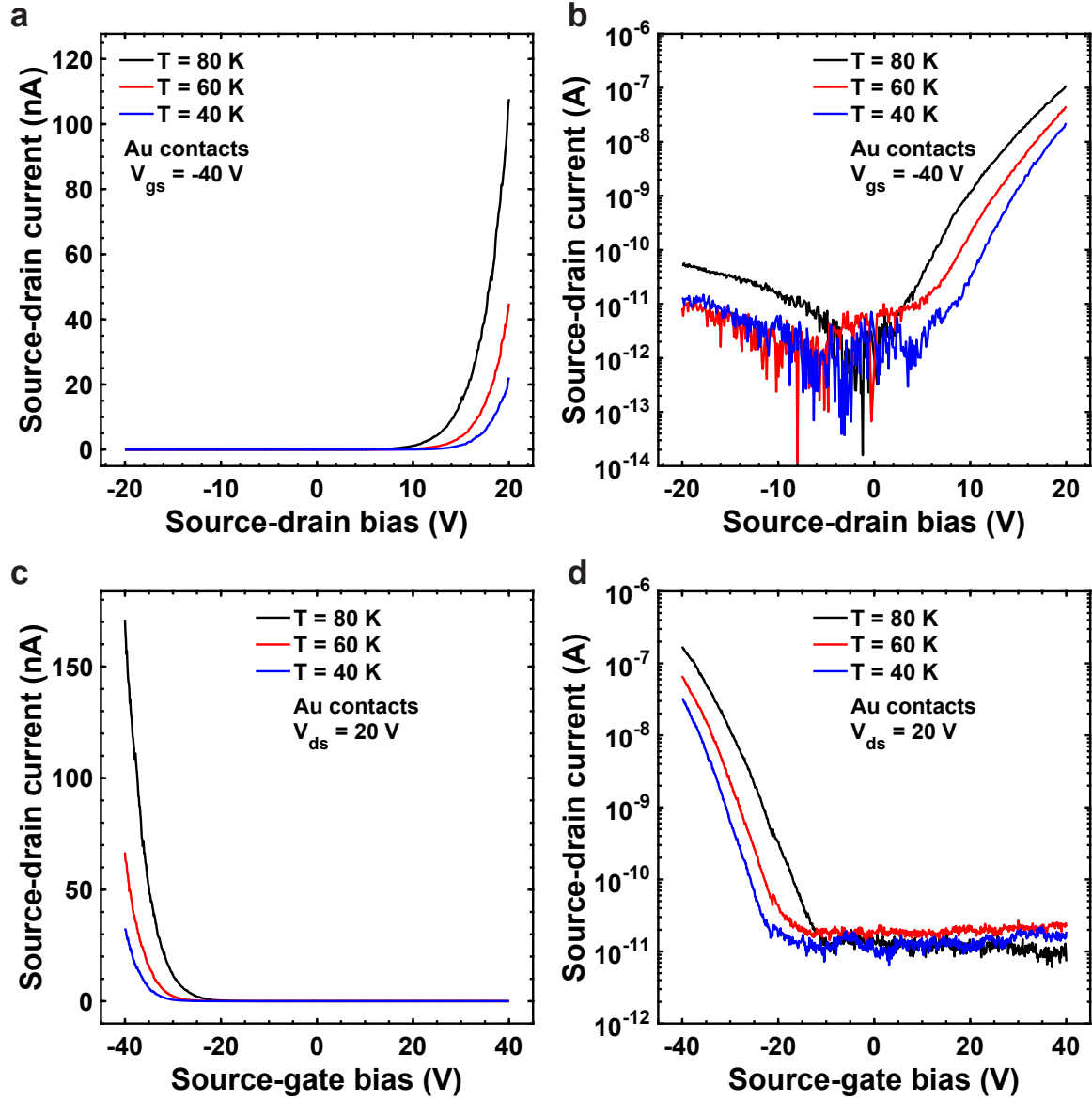


Figure 3. Electrical characterisation

a Response curves for a device with Au contacts at temperatures between 80 K and 40 K, measured with the devices in the “open” state at $V_{gs} = -40$ V. The curves exhibit a diode-like rectifying characteristics, as is further emphasised in the semi-logarithmic scale in **b**. **c** Transfer curves of the Au contacted device showing the characteristics of an enhancement type, *p*-channel semiconductor with a forward bias of $V_{ds} = +20$ V. The semi-logarithmic scale in **d** shows a constant current in the subthreshold region.

Fixing the source-drain bias to a “forward bias” configuration ($V_{ds} = +20$ V),

the source-drain current *vs* gate bias (I_{ds} - V_{gs}) transfer curves were measured, and are plotted in figure 3c. When the device is forward biased, it exhibits the characteristics of an enhancement type, *p*-channel transistor with its threshold voltage (V_{th}) growing increasingly negative with decreasing temperature. The semi-logarithmic scale plot, shown in figure 3d, shows the subthreshold region where the FET channel switches from its “closed” state to its “open” state and enters the linear regime. At 80 K, the two-terminal hole mobility extracted from the linear region of the transfer graph is around $0.1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, which is in agreement with our previously published devices,[24] but lower than the values reported by other groups.[25] We attribute the lower mobility to a high density of interface states, present either at the contacts or across the semiconducting flake. As we will show, this high density of traps contributes to the pinning of the Fermi level at the contacts and is instrumental in the realisation of ultra-low Schottky barriers. Other devices discussed in this report showed similar trends, see supplementary figure S2 online. Contrary to MoS₂,[26] in MoTe₂ *p*-type behaviour dominates the transistor characteristics among all the metals used, with the exception of Ti which induces an asymmetric ambipolar behaviour, with *p*-doping at $V_{gs} = 0 \text{ V}$.

The conductivity dependence on the temperature, determined by the response and transfer curves, which were acquired at different temperatures, reveals that the charge transport is dominated by a thermionic emission over an energy barrier. There are three main mechanisms of transport across an energy barrier: (1) thermionic emission from the high-end tail of Boltzmann distributed particles, (2) diffusion and (3) tunnelling (or field emission) through the barrier.[27, 11] For thermionic emission of charge carriers into a three-dimensional semiconductor, the current dependence with temperature (T) is given by the Schottky diode equation $I = AA^*T^2 \exp(-E_A/kT) [\exp(qV/nk_B T) - 1]$, where A is the contact area, $A^* = 4\pi m^* q k_B^2 / h^3$ is the modified Richardson constant, E_A is the activation energy required to overcome the barrier, n is the ideality factor, q is the basic charge and k_B is the Boltzmann constant. Other mechanisms of charge transport differ mainly in the exponent of T , which is 0 for diffusion and 1 for tunnelling. To determine the transport mechanism, the MoTe₂ FET current *vs.* temperature plot shown in figure 4a is fitted with $I_{ds} = B \cdot T^\alpha e^{-C/T}$, where α is the exponent of T used as a fitting parameter and B and C are arbitrary constants. The use of the pre-exponential constant is justified by plotting the current at different temperatures with fixed V_{ds} and fixed V_{gs} . The extracted $\alpha = 2.082 \pm 0.211$ is in good agreement with the temperature exponent for thermionic emission, suggesting that this is the dominant transport mechanism governing the transport in the device, while diffusion and tunnelling of charges play a negligible role in the temperature range between 40 K and 80 K. This is further supported by previous work that has shown the channel is depleted of its majority carriers,[24] leading to the formation of barriers as wide as $10 \text{ }\mu\text{m}$ in MoTe₂,[28] a fact which renders the efficiency of the tunnelling process insignificant. Further discussion on the additional transport mechanisms are included in supplementary information section III online.

For thermionic emission to occur at low temperatures the thermal width of the

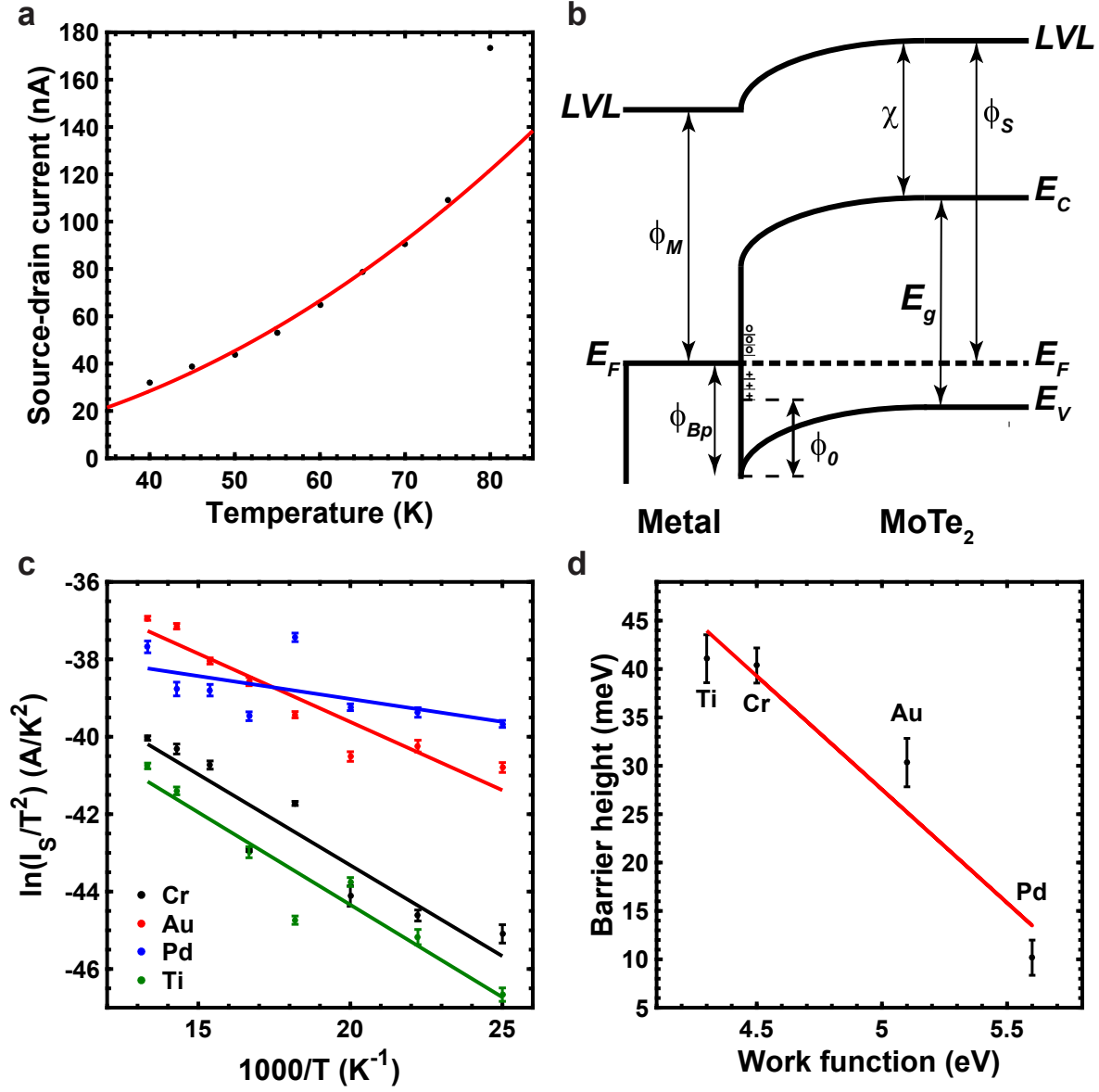


Figure 4. Barrier height determination

a Current-temperature dependence for an Au contacted device in the “open” state, showing a good agreement with the thermionic emission model for temperatures below 80 K. **b** Schematic energy band diagram of the metal/*p*-type semiconductor interface showing band bending of the conduction band edge E_C , the valence band edge E_V and the local vacuum level LVL when the Fermi levels E_F are aligned and the system is in thermal equilibrium. The metal work function ϕ_M , MoTe₂ work function ϕ_S , electron affinity χ , band gap E_g and barrier height ϕ_{Bp} are noted in the diagram. **c** A Richardson plot for the different devices at $V_{gs} - V_{th} = -11$ V. **d** The relation between barrier height and metal work function from which the extent of E_F pinning can be determined.

Fermi-Dirac distribution (ΔE) has to be comparable to or lower than the barrier height. ΔE for the majority (80%) of charge carriers can be found using the Fermi-Dirac distribution ($f(E) = 1/(1 + \exp((E - E_F)/k_B T))$)[27] by considering the region

between $f = 0.1$ and $f = 0.9$. Within this range, the thermal distribution width is given by $\Delta E = 4.4k_B T$. Supplementary figure S6 online shows the thermal distribution width as a function of temperature. Between the temperatures of 40 K and 80 K, the thermal distribution width ranges from 15 meV to 30 meV. When the thermal energy distribution grows larger than the barrier height, additional mechanisms of charge transfer over an energy barrier, such as tunnelling currents and diffusion, become more prominent, rendering the thermionic emission mechanism irrelevant at higher temperatures.

As previously discussed, the thermionic emission occurs over the source/channel energy barrier that forms when the Fermi energies of the semiconductor and metal reach thermal equilibrium. The surface potential of the metal depletes the adjacent segment of the channel, effectively bending the energy bands of the semiconductor, as shown in figure 4b, forming the Schottky barrier. In the ideal case the SBH (ϕ_{Bp}) is a function of the metal work function (ϕ_M), the semiconductor electron affinity (χ) and (for p -type materials) the band gap (E_g), given by the Schottky-Mott rule, $\phi_{Bp} = E_g + \chi - \phi_M$. [10] To tune the barrier height, four different metals were used for the contacts, Ti, Cr, Au and Pd with work functions of 4.3[13], 4.5,[29] 5.1[29] and 5.6 eV[30] respectively. These work functions should theoretically form barrier heights of 480, 280, -320 and -820 meV respectively, based on an electron affinity of 3.78 eV[31] and a band gap of 1.0 eV[32] for few-layer MoTe₂. Within this model a negative SBH is indicative of Ohmic contacts. In a realistic interface, mid-gap states, that may be formed by vacancies,[10] oxidation,[25] and MIGS,[33] increase the quantum capacitance of the band gap, an effect known as ‘‘Fermi level pinning’’, effectively altering the barrier height. In the extreme case, known as the Bardeen limit, a large density of mid-gap states can pin the barrier height completely.[10]

The MoTe₂ FET exhibits a diode-like behaviour, due to the pinned source/channel potential. As such, we may regard it as a single junction device, while treating the second junction as a fixed resistor. This point is further demonstrated in section II of the supplementary information online. In a single diode device, the height of the barrier can be extracted from temperature dependent transport measurements using a Richardson plot.[15] To this end the response curves are fitted with the diode equation $I_{ds} = I_S \exp(-q(V_{ds} - I_{ds}R_S)/nk_B T) - V_{ds}/R_P$, where R_S is a series resistance that includes the channel resistance and the contact resistance and R_P is a parallel shunt resistance. I_S is the saturation current which is given by $I_S = AA^*T^2 \exp(-\phi_{Bp}/k_B T)$ for thermionic emission. The extracted I_S values are then plotted as $\ln(I_S/T^2)$ vs $1/T$, shown in figure 4c and supplementary figure S7, which yield effective barrier heights of 41.1, 40.3, 30.3, and 10.2 meV for the Ti, Cr, Au and Pd contacts respectively.

The extraction of Schottky barrier heights as low as a few meVs can cause numerous difficulties due to competing mechanisms of transport. At low temperatures, thermionic field emission can be the dominant mechanism for charge injection into the channel.[34] However, our analysis of the source-drain current vs temperature at fixed source-drain bias and gate bias in figure 4a clearly show that thermionic emission is the dominant mechanism. In the determination of the barrier height, we used non-linear implicit

function fitting tool to allow the physical parameters I_S , R_S , R_P and n to reach a global minimum of residuals in the parameters space. For this, we have used a step-wise fit[35] to obtain the initial values of the parameters, which were then allowed to reach a higher degree of accuracy. Indeed, the largest source of error in the fittings came from the noise level of the instruments with the small current signal at the lower temperatures.

It is important to note two major consequences of the measured results. First, while the resulting trend is in excellent qualitative agreement with the theoretical case where the barrier height decreases with an increase in metal work function, the extracted effective barrier heights differ profoundly from the calculated values. This indicates significant pinning of the Fermi level by mid-gap states. Second, the measured Schottky barrier heights are comparable with the Fermi Dirac thermal distribution width, thus confirming that thermionic emission over an energy barrier is the dominant current mechanism.

The extent of Fermi level pinning can be quantified by comparing the barrier height with the metal work function using $\phi_{Bp} = \phi_0 + S(\phi_M - \phi_0)$, [10, 36] where ϕ_0 is the reference energy of the mid-gap states. The pinning factor S is equivalent to -1 in the ideal case with no pinning (Schottky limit) and 0 if E_F is completely pinned (Bardeen limit). Figure 4d shows that the linear decrease in effective barrier height with increasing metal work function, has a gradient of -0.02 that indicates very strong pinning of the Fermi level. From the intercept of the linear fit, the reference energy of the mid-gap states is found to be 0.14 eV above the valence band maximum. The strong pinning also means that gate tunability of the effective Schottky barrier height is considerably suppressed in these devices. Indeed, only the Au and Pd contacted devices show some tunability, exhibiting SBH modulation in the order of up to 40 meV for gate bias shifts of 15 V. This effect is most likely due to image force barrier lowering, and is discussed in further detail in supplementary figure S8 and the following discussion online in supplementary information Sec. VI, however further work needs to be carried out to fully elucidate this mechanism.

Considering the low charge carrier mobility and the strong Fermi level pinning, we attribute the measured effective barrier heights to the high density of mid gap states present at the metal/semiconductor interface. We have previously shown that slow charge carrier dynamics in MoTe₂ strongly affects the performance of FETs.[24] However, for photodetectors that are based on internal photoemission of charge carriers between the contact and the channel at that interface, the slow drift of charge carriers does not impede the performance of the detector, and can in fact serve as a short-lived reservoir for excited holes.

4. Conclusion

MoTe₂ FETs that exhibit ultra-low effective SBH were presented for the first time. The effective SBH can be controlled by changing the contact metal to some extent, but is dominated mainly by pinning of the Fermi level at the interface. The reference energy

of the mid-gap states, which is a measure of the highest energy of occupied mid-gap states, was found to be 0.14 eV above the valence band maximum. The tunability of the barrier may assist in the design of internal photoemission based photodetectors, particularly for near-infrared applications.

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Sub 20 meV Schottky barriers in metal/MoTe₂ junctions

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I Response and Transfer curves of other devices

The response and transfer curves for devices bearing Ti, Cr and Pd metal contacts exhibit a similar trend to the Au contacted devices with the diode-like behaviour in the response curve, and an enhancement type *p*-channel FET in the transfer. The device bearing Ti metal contacts exhibits amipolar behaviour in the transfer curves with the smaller metal workfunction. The plots are shown in Supplementary Fig. S1 and S2, respectively. The charge carrier mobilities were extracted from the linear regions of the I_{ds} - V_{gs} transfer curves at $T = 80$ K. and were found to be 0.01, 0.1 and 1.1 $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ for the Cr, Pd and Ti bearing devices respectively. These values are underestimated as two terminal measurements were used.

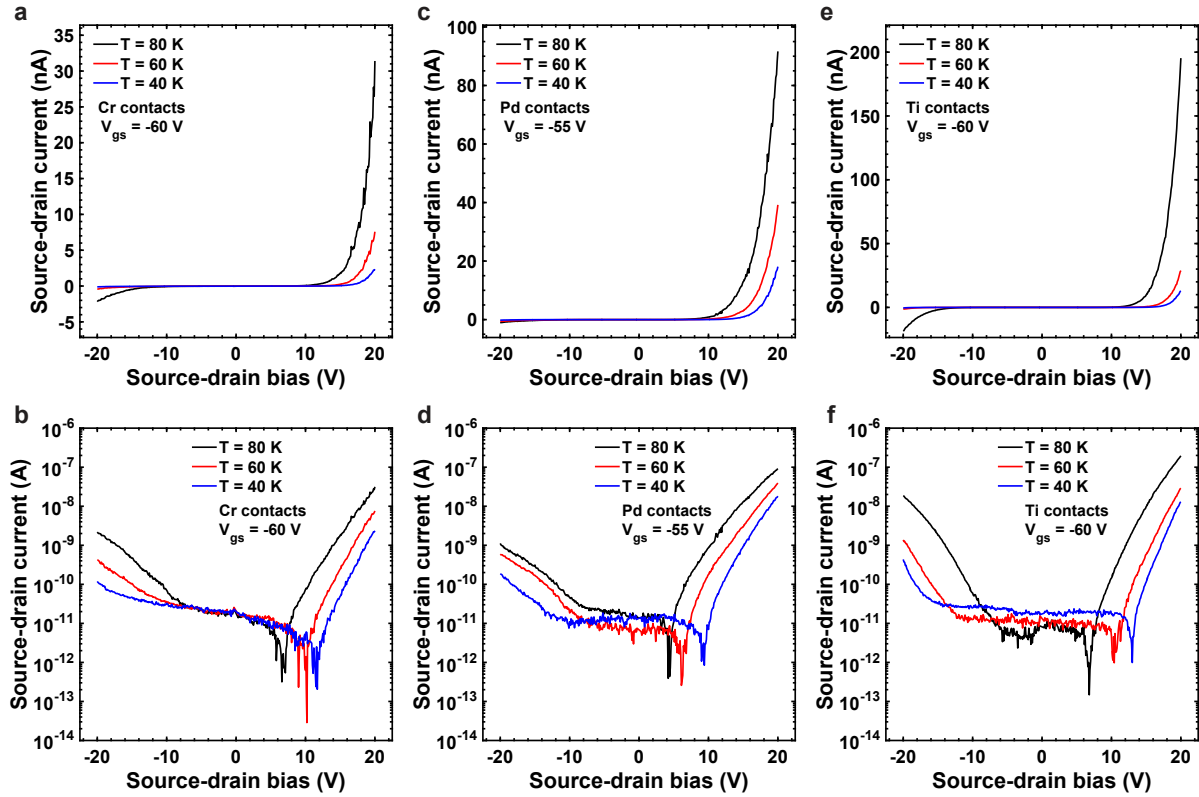


Figure S1: Response curves for metals with Cr (a,b), Pd (c,d), and Ti (e,f) contacts while the devices are in the “open” state. The top row (a,c,e) shows the plots on a linear scale and the bottom row (b,d,f) show the response curves on a semi-logarithmic scale.

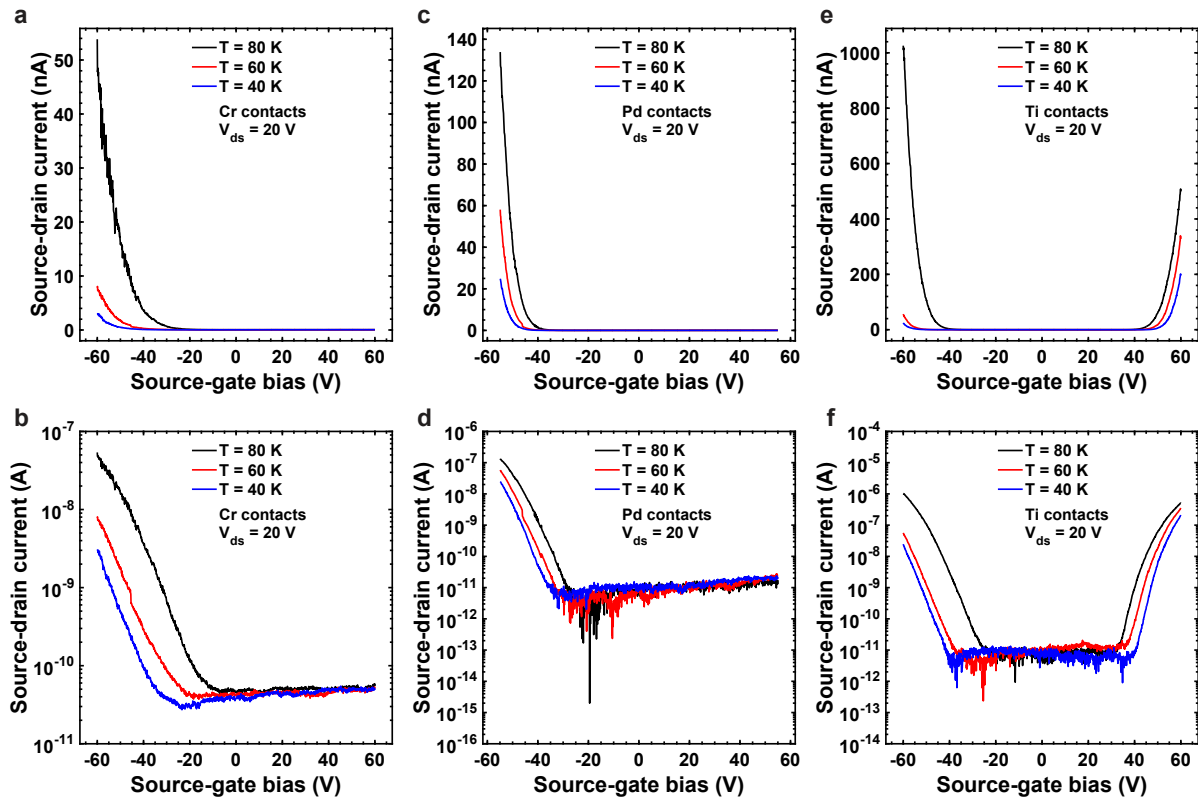


Figure S2: Transfer curves for FETs with Cr (a,b), Pd (c,d), and Ti (e,f) contacts while the devices are forward biased with $V_{ds} = +20\text{V}$. The top row (a,c,e) shows the plots on a linear scale and the bottom row (b,d,f) show the response curves on a semi-logarithmic scale.

II Pinning of source electrode

For the analysis shown in this report, the source electrode is assumed to be pinned at the contact to the extent that it can be considered as a constant resistor, and the gate modulation only affects the forward bias direction. This analysis is fundamentally different from the intuitive back-to-back diode architecture that should be present in the case of an unpinned interface. To justify our assumption of one “diode” being pinned we qualitatively compare our measured data to numerical models of a single diode and two back-to-back diode model in Supplementary Fig. S3.

The response curves at 80 K at different gate biases are shown in Supplementary Fig. S3a. To address the results with a correct model, two simplified cases were considered and solved numerically using the Trust-Region Dogleg algorithm (Newton Method) on Matlab. The first case is a single diode model¹ and was solved using a system of equations of the form:

$$I = I_S \left[\exp \left(\frac{q(V_J - IR_s)}{nk_B T} \right) - 1 \right] \quad (\text{S1a})$$

$$V_A = IR_s + V_J \quad (\text{S1b})$$

Where I is the current, I_S is the saturation current, q is the elementary charge, V_J is the potential drop over the junction, R_s is the series resistor that includes the “second” (non-dynamic) diode, n is the ideality factor, k_B is the Boltzmann constant, T is the temperature and V_A is the applied bias. To reflect the changes in junction conductivity with gate modulation, the value of I_S in the model was reduced at high gate bias. This change is in accordance with the images charge barrier lowering model that is discussed in details in Supplementary Information Sec. VI.

The second case that was considered is the case of two back-to-back diodes,¹ where the device was modelled using the following system of equations:

$$I = I_S^{(1)} \left[\exp \left(\frac{q(V_1 - IR_s)}{nk_B T} \right) - 1 \right] \quad (\text{S2a})$$

$$I = I_S^{(2)} \left[1 - \exp \left(\frac{q(IR_s - V_2)}{nk_B T} \right) \right] \quad (\text{S2b})$$

$$V_A = IR_s + V_1 + V_2 \quad (\text{S2c})$$

Where $I_S^{(i)}$ is the saturation (reverse) current of the i^{th} ($i = 1, 2$) junction, and V_i is the voltage drop on the i^{th} junction.

Comparing the experimental curve to the single diode model (Supplementary Fig. S3b) and the two diode model (Supplementary Fig. S3c), it is clear that the measured data agrees with the single-diode case.

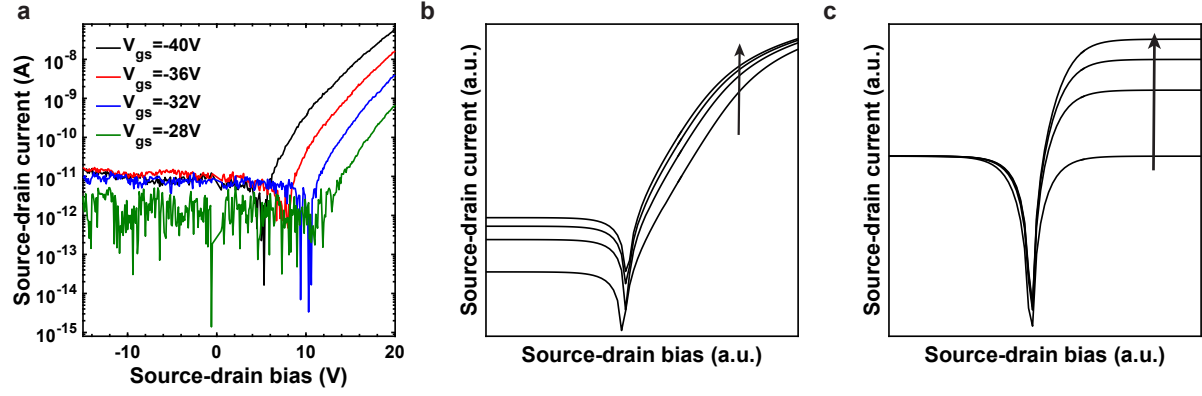


Figure S3: A comparison of the response curves of an Au bearing device at 80 K at various gate bias values (a) to calculated response curves of a single diode with a series resistor model (b) and those of two back-to-back diodes model (c).

III Transport mechanisms over an energy barrier

When injecting a current over an energy barrier, the three main injection mechanisms differ in their dependence on the temperature. For diffusion, the saturation current dependence on the temperature (T) is $I_D \propto \exp(-q\phi_{Bp}/k_B T)$, where q is the elementary charge, ϕ_{Bp} is the barrier height, and k_B is Boltzmann's constant. For field emission (tunnelling), the current is given by $I_{FE} \propto T \exp(-q(\phi_{Bp} - V_{ds})/E_{00})/\sin(\pi c_1 k_B T)$, where $c_1 = (1/2E_{00}) \log(4(\phi_{Bp} - V_{ds})/\phi_p)$, $E_{00} = q\hbar\sqrt{N/4m^*\epsilon_s}$, \hbar is the reduced Planck's constant, m^* is the effective mass of the charge carrier, and N is the doping concentration. Finally, for thermionic emission, $I_S \propto T^2 \exp(-\phi_{Bp}/k_B T)$. From the three models, the difference in temperature dependence for each of the mechanisms arises from the exponent of the temperature in the pre-exponential factor.¹

The fitting curves for devices bearing Cr, Pd and Ti contacts are presented in Supplementary Fig. S4 and found to be in good agreement with the thermionic emission model, up to 80 K.

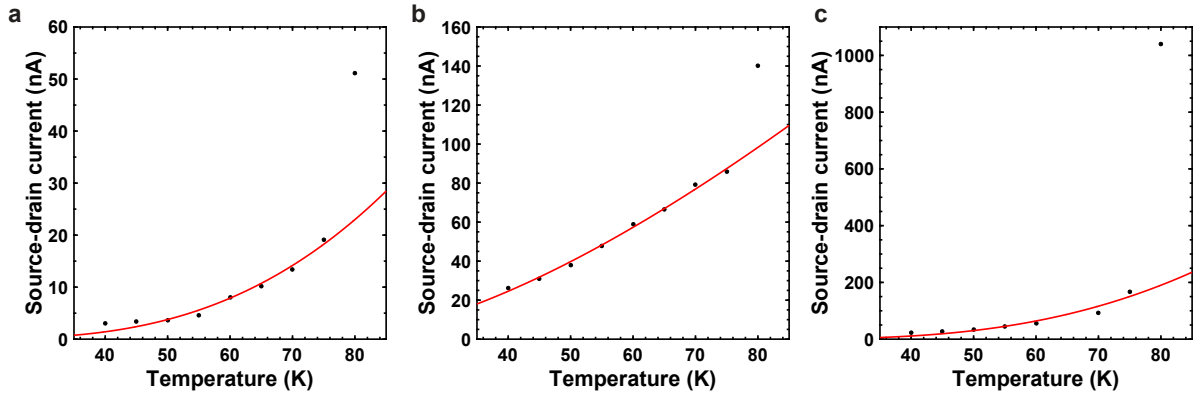


Figure S4: Current vs. temperature fittings for Cr (a), Pd (b) and Ti (c) with fits showing $\alpha_{Cr} = 2.571$, $\alpha_{Pd} = 2.081$ and $\alpha_{Ti} = 2.281$ at temperatures below 80 K.

For the device bearing Au contacts, the temperature dependence on source-drain current was also examined at different gate biases within the linear regime of the $I_{ds} - V_{gs}$ transfer curves, shown in Supplementary Fig. S5a. The fittings showed the temperature exponent of approximately 2 for the three values of V_{gs} , indicating thermionic emission is still the dominant mechanism.

For a different device bearing Pd contacts, these measurements were repeated over a wider temperature

range of 80 K to 300 K and is shown in Supplementary Fig. S5b. In this case, the fitting curves exhibited a mixed dependence on thermionic emission and tunnelling with $\alpha = 1.5424$, suggesting tunnelling contributions become significant at higher temperatures. As discussed in the main text and in more detail in Supplementary Information Sec. IV, this is in agreement with the thermal width of the charge carriers being greater than the measured barrier height, and therefore allowing tunnelling to occur. Also, with tunnelling being a significant contributor to transport over the barrier, thermionic emission in this temperature range cannot be solely used to determine barrier height, and is outside the scope of this work.

A qualitative measure of the contribution from each of the transport methods can be determined by comparing $k_B T$ to E_{00} . When $E_{00} \ll k_B T$, thermionic emission (TE) is dominant, whilst tunnelling (FE) is the main contributor to transport through the barrier when $E_{00} \gg k_B T$. If $E_{00} \approx k_B T$, a combination of both thermionic emission and tunnelling (TFE) occurs. This is illustrated in Supplementary Fig. S5c, where theoretical values for MoTe₂ of $m^* = 0.3m_e$ and $\epsilon = 8$ were used.² This shows that for tunnelling to be a significant contributor to the transport across the barrier, the MoTe₂ would need to be highly doped to a carrier concentration above 10^{18} cm^{-3} , which is unlikely based on the presence of a high density of charge traps within the channel.³ Therefore, at temperatures below 80 K, fitting of thermionic emission to $I_{ds} - V_{ds}$ response curves can be used to extract the barrier height.⁴ However, further work needs to be carried out to quantise the doping concentration in MoTe₂, which is outside the scope of this paper.

Based on this model, the doping concentration should have increased to allow the significant contribution from tunnelling observed at temperatures between 80 K and 300 K. At the higher temperatures, the Fermi-Dirac distribution shows the thermal width becomes greater than the barrier height, as discussed in further detail in Supplementary Information Sec. IV. This would then cause tunnelling to become more important. However, further investigations need to be carried out to explain the increase in tunnelling at higher temperatures.

The alignment of the Fermi level across the metal/semiconductor at thermal equilibrium results in band bending on the semiconductor side. The lateral width over which the energy bands are bent, called the depletion width W_D , has a significant effect on the tunnelling probability, which decreases exponentially with W_D , as is shown schematically in Fig. S6. At low temperatures, the charge carriers have low energy with a narrow

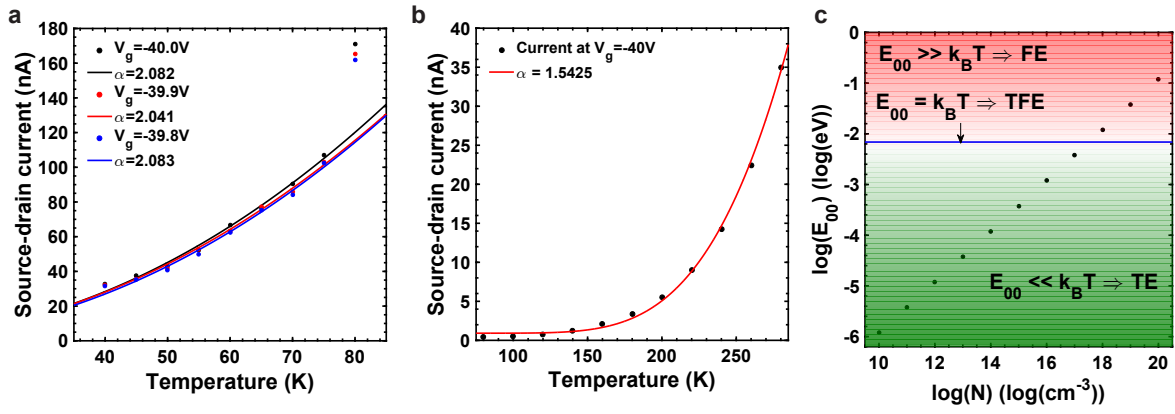


Figure S5: **a** Current vs temperature fittings for Au at different gate biases within the linear regime showing $\alpha_{V_g=-40.0V} = 2.082$, $\alpha_{V_g=-39.9V} = 2.041$ and $\alpha_{V_g=-39.8V} = 2.083$ at temperatures below 80 K. **b** Current vs temperature fittings for Pd over a wider temperature range with a fit showing $\alpha_{highT} = 1.5425$, suggesting tunnelling contributions become more significant at higher temperatures. **c** Relative contributions of thermionic emission (TE) when $E_{00} \ll k_B T$, tunnelling (FE) in the region $E_{00} \gg k_B T$ and a combination of both (TFE) when $E_{00} \approx k_B T$.

distribution, resulting in a wide effective barrier which significantly reduces the probability of tunnelling is smaller than at higher temperatures. In the case of MoTe₂, the depletion width has been calculated to be of the order of 10 μm ,⁵ practically nullifying the probability for tunnelling. However, since the barrier height requires an energy which is comparable to the Fermi-Dirac thermal spread, charge injection into the channel can still occur by thermionic emission over the barrier.

IV Fermi-Dirac Distribution curves

The Fermi-Dirac distribution shows the occupancy of states at energy E , as a function of temperature T and the Fermi energy E_F :¹

$$F_{FD}(E) = \frac{1}{1 + \exp[(E - E_F)/k_B T]}, \quad (\text{S3})$$

A plot of the Fermi-Dirac distribution at an arbitrary finite temperature is shown in Supplementary Fig. S7a.

Considering the majority (80 %) of charge carriers that are available for thermionic emission, we need

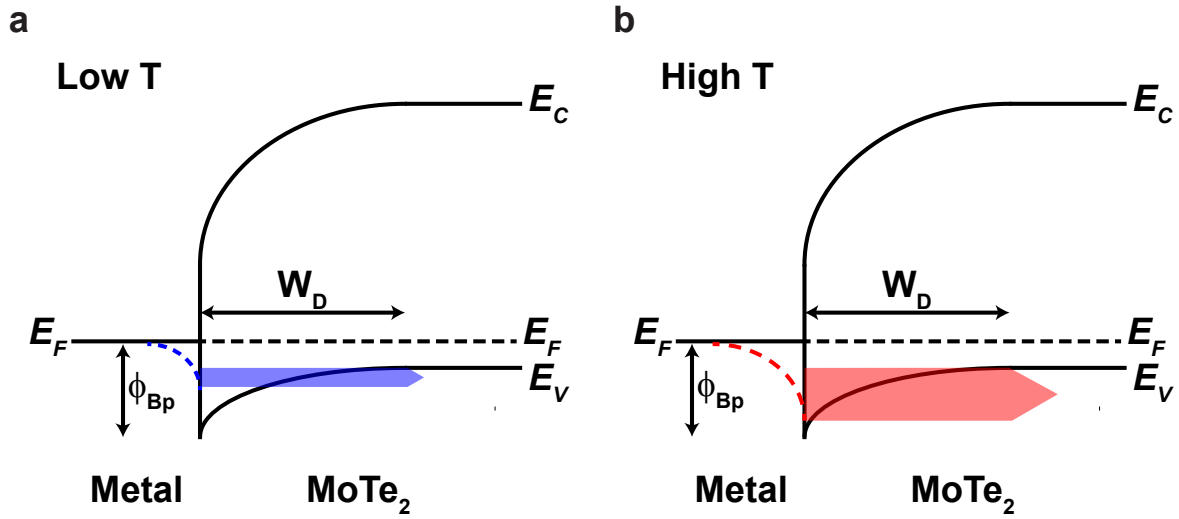


Figure S6: Schematic of the band bending caused by the formation of a Schottky barrier at the interface between a metal contact and the MoTe₂ channel showing the depletion width. At low temperatures (a) the depletion width associated with the low energy of the charge carriers is longer than that for the high temperature case (b) and, therefore, the tunnelling efficiency is lower.

to determine the thermal width ΔE which is in the range of energies bounded by $f_1 = F_{FD}(E_1) = 0.1$ and $f_2 = F_{FD}(E_2) = 0.9$. The charge carriers in this range are given by:¹

$$\Delta E = kT \ln \left(\frac{0.81}{0.01} \right) \simeq 4.4kT \quad (\text{S4})$$

The thermal width is linear with temperature and is plotted in Supplementary Fig. S7b, accounting for only thermally excited particles ($E < E_F$ for holes) it is clear that the thermal distribution width is of the same order of magnitude as the measured SBHs, supporting our observation that the charge injection mechanism is indeed thermionic emission, at the relevant temperatures (< 80 K).

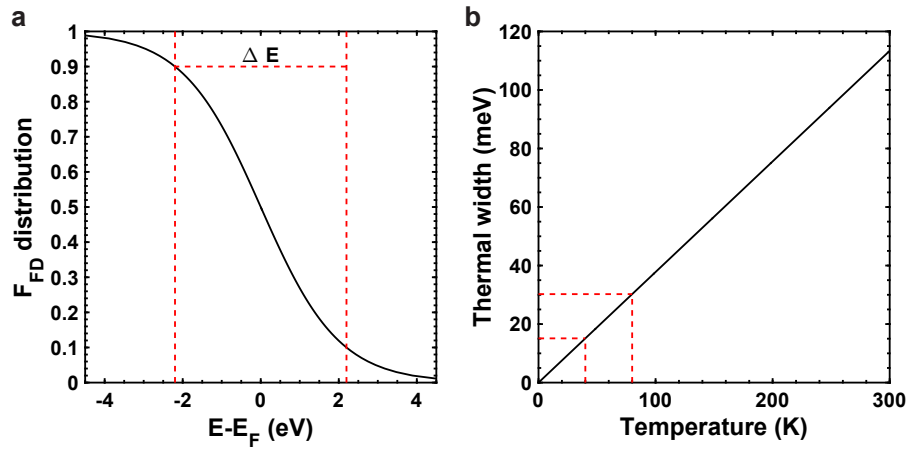


Figure S7: The Fermi-Dirac distribution at an arbitrary finite temperature (a) with the majority (80%) of charge carriers are in the range $f_{FD} = 0.1$ and $f_{FD} = 0.9$ shown by the red dashed line. This thermal width follows the temperature linearly as is shown in (b).

V Barrier height for each device at different gate biases

Further experimental results showing the Richardson plot for tested devices with all types of metal contacts used in this work are shown in Supplementary Fig. S8

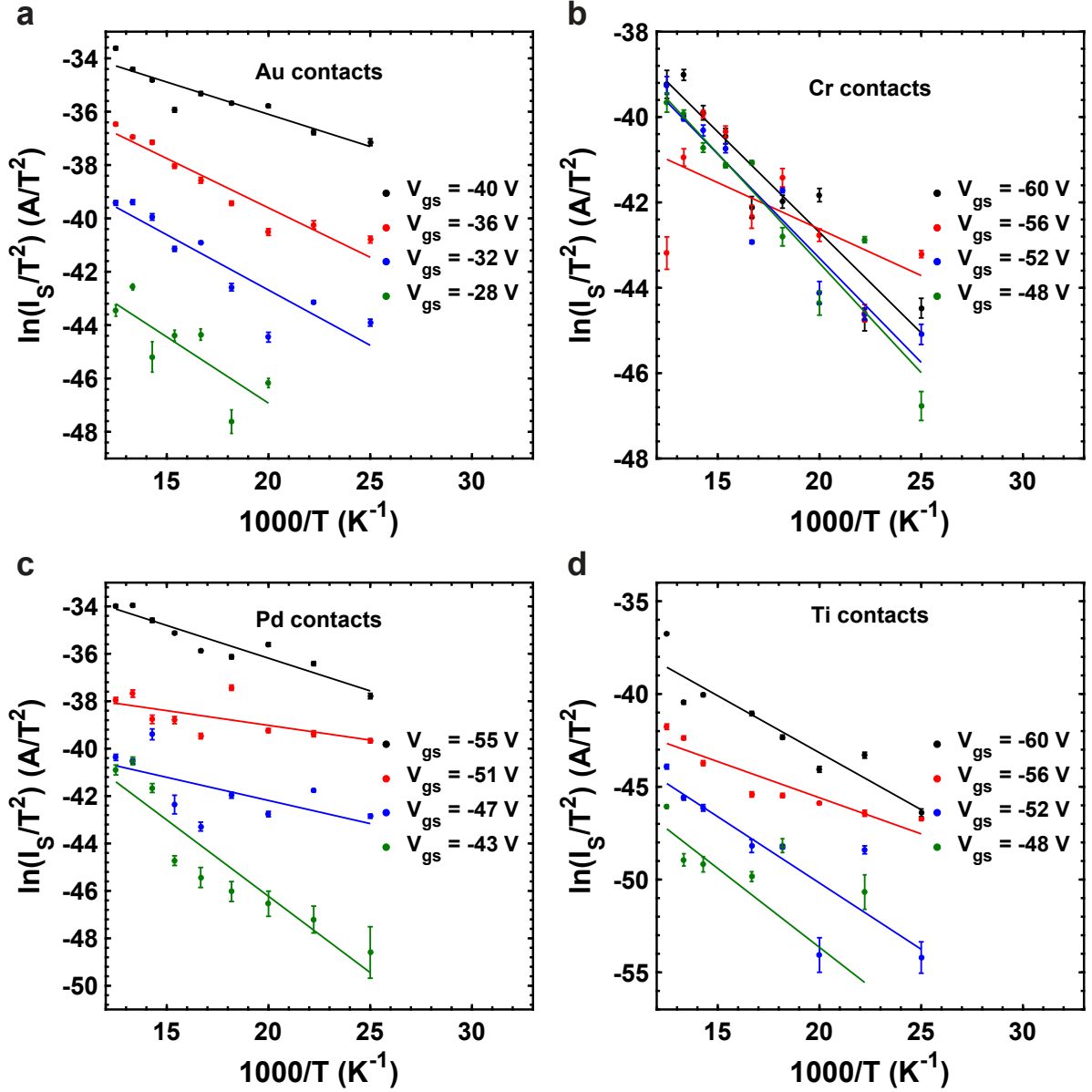


Figure S8: Richardson plots for the various gate voltages for Au (a), Cr (b), Pd (c) and Ti (d) showing similar trends.

VI Gate tuneability of Schottky barriers

Gate modulation of the effective barrier height was observed for the Au and Pd contacted devices, as shown in Supplementary Fig. S9a. This tuneability is most likely due to image force barrier lowering¹ where the SBH is reduced from its equilibrium value ϕ_{Bp0} by $\Delta\phi$ in the presence of an electric field, such as that provided by the gate bias. By shifting the Fermi level towards the valence band, the depletion region becomes smaller as

more free charge carriers are accumulated in the MoTe₂ channel. However, the voltage drop over the junction remains constant, resulting in a larger electric field over the depletion region which reduces the effective barrier height. There was no gate modulation observed for the Cr and Ti contacted devices, shown in Supplementary Fig. S9b. Supplementary Fig. S9c shows schematically two band diagrams, one for a low gate bias (solid) and one for a higher bias value (dashed). These diagrams demonstrate the effect that a shift of the Fermi level has the depletion width (W_{D1} and W_{D2}), which in turn changes the effective SBH by lowering the equilibrium barrier by $\Delta\phi_i$.

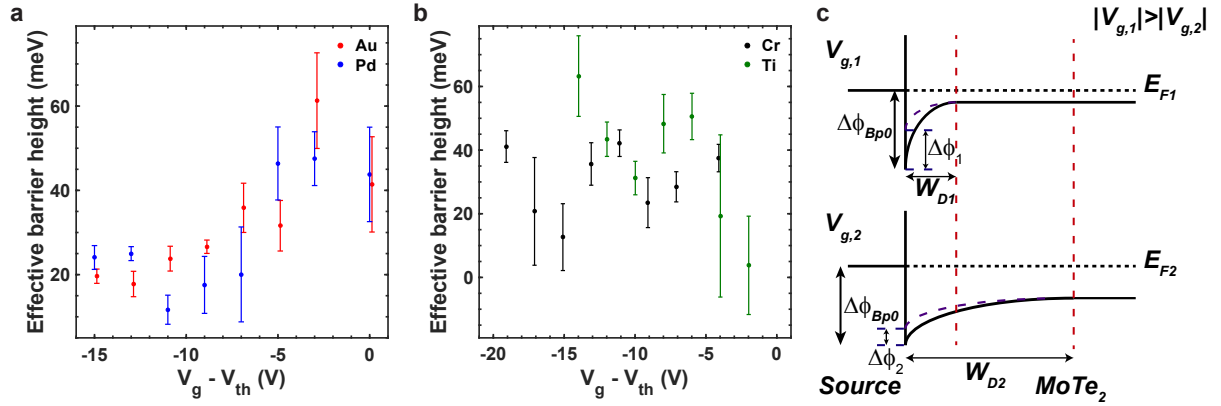


Figure S9: The effective Schottky barrier height at different gate biases for Au and Pd (a) shows a slight trend expected to be the result of image-force barrier lowering, as is shown in the schematic band diagram in c, whilst the effective barrier height appears to follow no such trend for the devices bearing Cr and Ti contacts (b).

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